Claims:

1. A microcontroller architecture comprising:

a processor (101) for processing of instruction data comprising memory access instructions for accessing of a memory circuit (105);

at least a pointer memory circuit (103a, 103b, 103c, 103d) for storing of a pointer address forming part of the instruction data;

at least a pointer register (200a, 200b, 200c, 200d) for storing a duplicate of the pointer address; and,

a control circuit (102) for determining whether one of a read operation from the at least a pointer memory circuit (103a, 103b, 103c, 103d) and a write operation to the at least a pointer memory circuit (103a, 103b, 103c, 103d) is to take place, wherein for a write operation the control circuit (102) stores the pointer address in the at least a pointer memory circuit (103a, 103b, 103c, 103d) and automatically stores a duplicate in the at least a pointer register (200a, 200b, 200c, 200d) and where for a read operation the control circuit utilizes the at least a pointer register (200a, 200b, 200c, 200d) to access data pointed to by a target pointer address derived from the pointer address stored therein and other than accesses the at least a pointer memory (103a, 103b, 103c, 103d).

2. A microcontroller architecture according to claim 1, comprising a pointer multiplexer block (300) having at least an input port coupled to the at least a pointer register (200a, 200b, 200c, 200d) for receiving a pointer address and an output port for providing the pointer target address used for indirect addressing operations of data stored within the memory circuit (105).

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3. A microcontroller architecture according to claim 2, comprising a source select block (600) having a first input port for receiving a next program address derived from a current program counter value plus a length of a current instruction, a second input port for receiving the pointer target address from the pointer multiplexer block (300), a third input port for receiving a selection signal from the control circuit (102) for determining which data bits from the at least one of the input signals received at the first and second input ports are to be used for providing of pointer data output signals from output ports of the source select block (600).

4. A microcontroller architecture according to claim 3, wherein the at least a pointer register (200a, 200b, 200c, 200d) comprises a plurality of pointer registers (200a, 200b, 200c, 200d), the microcontroller architecture comprising an input multiplexer (400) having input ports coupled to the output ports of the source select block (600) for receiving of the pointer data output signals therefrom, and for receiving of an input data multiplexer control signal from the control block (102), the input multiplexer control signal for determining which data bits derived from the pointer data output signals are to be used in forming of the pointer address for storage in the plurality of pointer registers (200a, 200b, 200c, 200d).

5. A microcontroller architecture according to claim 4, wherein the at least a pointer memory circuit (103a, 103b, 103c, 103d) comprises a plurality of pointer memory circuits (103a, 103b, 103c, 103d), the microcontroller architecture comprising an output multiplexer (500) having input ports coupled to plurality of pointer memory circuits (103a, 103b, 103c, 103d) for receiving of data bits derived from the stored pointer address stored within the plurality of pointer memory circuits (103a, 103b, 103c, 103d) and having an output port for providing a program counter value for being restored during a return from interrupt instruction.

6. A microcontroller architecture according to claim 5, wherein the pointer multiplexer (300) and the output multiplexer (500) and the input multiplexer (400) are other than clock circuit gated.

7. A microcontroller according to claim 1, comprising a clock circuit (104) having a clock cycle and coupled to the at least a memory circuit (105), the at least a pointer register (200a, 200b, 200c, 200d), and the control block (102), wherein the read operation accesses a region in the memory circuit (105) that is addressed by the target pointer address within a single clock cycle.

8. A method of pointer based addressing comprising the steps of:

providing at least a pointer memory (103a, 103b, 103c, 103d);

providing at least a pointer register (200a, 200b, 200c, 200d);

storing of a pointer address data in the at least a pointer memory (103a, 103b, 103c, 103d); and,

upon storing (701) of a pointer address data in the at least a pointer memory (103a, 103b, 103c, 103d), automatically storing a duplicate pointer address data, which is a duplicate of the pointer address data, in the at least a pointer register (200a, 200b, 200c, 200d).

9. A method according to claim 8, wherein the step of automatically storing is performed within a same clock cycle as the step of storing.

10. A method according to claim 8, wherein the step of automatically storing is performed after the step of storing such that the at least a pointer memory (103a, 103b, 103c, 103d) is other than accessible by other operations until the step of automatically storing is completed.

11. A method according to claim 8 comprising the step of detecting all changes to the at least a pointer memory (103a, 103b, 103c, 103d) for automatically storing the duplicate pointer address data.

12. A method according to claim 8, comprising the steps of:

receiving (702) a memory access request to a memory location within a memory for retrieving of data stored at the memory location addressed by the pointer address;

retrieving (703) of the duplicate pointer address data from the pointer register; and,

accessing (704) the memory using a target pointer address derived from the duplicate pointer address data and other than using a target pointer address derived from the pointer address data stored in the at least a pointer memory.

13. A method according to claim 12, comprising the step of providing a clock circuit (104) having a clock cycle, wherein the steps of receiving (702), retrieving (703) and accessing (704) are performed in a single clock cycle.

14. A method according to claim 12, comprising the step of writing back the target pointer address to the at least a pointer register (200a, 200b, 200c, 200d) and to the at least a pointer memory (103a, 103b, 103c, 103d).

15. A method according to claim 12, comprising the step of detecting all changes to the at least a pointer memory (103a, 103b, 103c, 103d) for automatically storing the duplicate pointer address data.

16. A method according to claim 12, wherein the at least a pointer register (200a, 200b, 200c, 200d) comprises a plurality of pointer registers (200a, 200b, 200c, 200d), wherein the step of accessing comprises the step of multiplexing of the pointer address data stored in the plurality of pointer registers (200a, 200b, 200c, 200d) to form the target pointer address for accessing of the random access memory (105).

17. A storage medium having data stored thereon, the data for implementation of a processing system comprising:

first instruction data for providing at least a pointer memory (103a, 103b, 103c, 103d);

second instruction data for providing at least a pointer register (200a, 200b, 200c, 200d);

third instruction data for upon storing of a pointer address in the at least a pointer memory (103a, 103b, 103c, 103d), automatically storing a duplicate pointer address, which is a duplicate of the pointer address, in the at least a pointer register (200a, 200b, 200c, 200d);

fourth instruction data for receiving a memory access request to a memory location within a memory (104) for retrieving of data stored at the memory location addressed by the pointer address;

fifth instruction data for retrieving of the duplicate pointer address from the at least a pointer register (200a, 200b, 200c, 200d); and,

sixth instruction data for accessing the memory (104) using a target pointer address derived from the duplicate pointer address and other than using a target pointer address derived from the pointer address stored in the at least a pointer memory (103a, 103b, 103c, 103d);.